said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first side wall;

an erase gate formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said second one of said side walls by said second insulation layer;

a drain region formed in a portion of said substrate proximate said control gate; and

a source region formed in a portion of said substrate proximate said erase gate.

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8. (Once Amended) A memory array disposed on a substrate comprising a plurality of memory cells each having a floating gate separated from said substrate by a first insulating layer, an erase gate, a control gate separated from said floating gate by a second insulating layer, a source region, and a drain region, comprising:

a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same row are connected by a common word-line, the erase gates of the memory cells in the same rows are connected by a common erase line, the source regions of the memory cells in the same rows are connected by a common source line, and the drain regions of memory cells in the same columns are commonly connected via a common drain line, wherein at least a portion of each said control gate is disposed over a portion of said substrate and separated therefrom by said second insulating layer, and wherein a portion of said control gate is not disposed over said floating gate; and

control circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array.

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16. (Once Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said substrate and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first side wall;

an erase gate formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said second one of said side walls by said second insulation layer;

a source region formed in a portion of said substrate proximate said erase gate; and

a drain region formed in a portion of said substrate proximate said control gate.